Initially, Applicant respectfully requests withdrawal of the finality of the present Office Action. In the statement of the rejection, the Examiner cited M.P.E.P. § 706.07(a) as the basis for making the present Office Action final and stated: "Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action." However, M.P.E.P. § 706.07(a) clearly states:

> A second or any subsequent action on the merits in any application ... should not be made final if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should *reasonably* have been expected to be claimed. (emphasis added)

In the Amendment filed April 9, 2002, independent claims 1 and 10 were only amended to recite "said second buried impurity region includes a first gap part" instead of the originally claimed limitation of "said second buried impurity region includes a first recessed part ... *or* a first gap part." Put shortly, claims 1 and 10 were amended to recite "B" instead of "A or B." It is reasonable to expect that claims 1 and 10 would be amended by Applicant to recite "B" instead of "A or B," particularly when the Examiner cites a reference that discloses "A" but not "B." As the Examiner has cited a reference not of record to disclose the claimed first gap part, under M.P.E.P. § 706.07(a), the present Office Action should not have been made final, and therefore, Applicant respectfully solicits withdrawal of the finality of the present Office Action.

Claims 2-3 and 11 are rejected under the first paragraph of 35 U.S.C. § 112

In the second enumerated paragraph of the Office Action, the Examiner asserted that claims 2-3 and 11 contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. This rejection is respectfully traversed.

In the statement of rejection, the Examiner stated: "it is physically impossible for any electrodes parts formed on the surface of said semiconductor layer to be configured as to cause the first impurity regions to be sandwiched between it [?] and the third semiconductor region." Applicant notes, however, that neither claim 2 nor claim 11 recites that the first impurity region is between an electrode part and the third semiconductor region. The Examiner is also directed to the second paragraph on page 10 of the disclosure, in which the limitations of claims 2 and 11 are described and find full support (compare last line of the second paragraph of page 10 with last clause of claims 2 and 11, as originally presented). As such, Applicant respectfully submits that the specification fully supports these limitations in such a way as to enable one skilled in the art to make and/or use the invention.

Claims 1, 4 and 9 are rejected under 35 U.S.C. § 103 for obviousness predicated upon Ueno et al., U.S. Patent No. 5,895,939 (hereinafter Ueno), in view of Hwang et al., EP-0252173 A1 (hereinafter Hwang)

In the second enumerated paragraph of the Office Action, the Examiner asserted that Ueno discloses all of the claimed structure except for the first impurity region of a second conductivity type to be electrically connected to a second buried impurity region. The Examiner then asserted that "it would have been obvious to prevent the possibility of breakdown due to parasitic capacitance between regions 65, 63, and 70" and cited Hwang for this teaching. This rejection is respectfully traversed.

Initially, Applicant notes that claim 1 has been amended to recite that the gap part is positioned directly beneath the second impurity region. See, for example, Fig. 7 of Applicant's

disclosure, which shows a gap part 65 directly beneath a second impurity region (N diffusion region 8). In so doing, the invention provides improved breakdown voltage between the second impurity region (N diffusion region 8) and the second buried impurity region (P+ buried region 4) positioned below.

In the statement of the rejection, the Examiner identified feature 70 as a second buried impurity region, feature 65 as a first impurity region, and feature 64 as a second impurity region. In contrast to the recited, however, there is no gap portion of the second buried impurity region 70 of Ueno formed directly below the second impurity region 64. Instead, as illustrated in Fig. 6 of Ueno, the gap portion of the second buried impurity region 70 is formed below the first impurity region 65.

The semiconductor device of Ueno is a vertical JFET transistor operated by controlling the JFET formed between the first impurity region 65 and the second buried impurity region 70. Therefore, <u>if</u> the second impurity region 64 is arranged directly above the gap part of the second buried impurity region 70, as recited in claim 1, the structure of the JFET would be lost, and transistor operation could not be obtained.

Furthermore, Applicant notes that the Examiner's citation of Hwang fails to comport to the provisions of 37 C.F.R. § 1.104(c).[1] In particular, the Examiner neither <u>clearly</u> designated the

[1] 37 C.F.R. § 1.104(c) provides:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

teachings in Hwang being relied upon by the Examiner nor clearly explained the pertinence of Hwang. The Examiner's identification of "Example 1, page 17" is not a clear designation of the teachings being relied upon by the Examiner. As a result of the Examiner failing to clearly designate the teachings in Hwang being relied upon, Applicant is unable to identify the particular teachings in Hwang that allegedly provide the Examiner's asserted motivation to combine Hwang with Ueno.

The Examiner's assertion that electrically connecting feature 65 to feature 70 of Ueno, as taught by Hwang, would solve the parasitic capacitance problem fails to consider the fatal consequence of the Examiner's suggestion. Electrical capacitance between two features, as opposed to electrical conductance, occurs because the features are intended to be separated from one another. However, by connecting feature 65 to feature 70 of Ueno, the Examiner has introduced a short into the circuit of Ueno. Therefore, one having ordinary skill in the art would not have been motivated to modify Ueno to electrically connect feature 65 to feature 70. Therefore, Applicant respectfully solicit the withdrawal of the imposed rejection of claims 1, 4 and 9 under 35 U.S.C. § 103 for obviousness predicated upon Ueno in view of Hwang.

Claims 6 and 7 are separately rejected under 35 U.S.C. § 103 for obviousness predicated upon Ueno in view of Hwang, and further in view of Hirano, EP 0817387 A1, or alternatively, in view of Lin et al., U.S. Patent No. 6,348,714 (hereinafter Lin)

In the third and fourth enumerated paragraphs of the Office Action, the Examiner asserted that one having ordinary skill in the art would have been motivated to modify the combination of

Ueno and Hwang with either Hirano or Lin to arrive at the limitations recited in claims 6 and 7. This rejection is respectfully traversed.

Claims 6 and 7 depend ultimately from independent claim 1, and Applicants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. § 103 for obviousness predicated upon Ueno in view of Hwang. The secondary references to Hirano and Lin do not disclose the concept of a gap part that is positioned directly beneath the second impurity region. Accordingly, the proposed combination of references would not yield the claimed invention.

Furthermore, the Examiner's citation of Hirano and Lin are misplaced. Hirano appears to be directed solely to circuit arrangements and is completely silent with regard to the number of gap parts in a second buried impurity region. It is also particularly notable that Hirano discloses not one side view of the semiconductor device. As such, how could one having ordinary skill in the art evaluate the teachings of Hirano so as to modify Ueno and Hwang?

With regard to Lin, the Examiner merely states that Lin teaches "a plurality of buried impurity regions 116 separated by gaps so as to combat body effects such as kink effect." The Examiner, however, has failed to recognize that these effects, as stated in column 1, lines 28-37, are a result of a "floating substrate of MOS transistor formed on SOI." As neither Ueno or Hwang involve silicon on insulator (SOI), why would one having ordinary skill in the art solve problems related to a structure that is not present in the primary reference? Thus, Applicant respectfully

solicit the withdrawal of the imposed rejection of claims 6 and 7 under 35 U.S.C. § 103 for obviousness predicated upon Ueno in view of Hwang and further in view of Hirano or Lin.

Claim 8 is rejected under 35 U.S.C. § 103 for obviousness predicated upon Ueno in view of Hwang, and further in view of Galbiati et al., U.S. Patent No. 5,629,558

In the fifth enumerated paragraph of the statement of the rejection, the Examiner asserted that one having ordinary skill in the art would have been motivated to modify the combination of Ueno and Hwang with Galbiati to arrive at the limitations recited in claims 8. This rejection is respectfully traversed.

Claim 8 depends ultimately from independent claim 1, and Applicants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. § 103 for obviousness predicated upon Ueno in view of Hwang. The secondary reference to Galbiati does not disclose the concept of a gap part that is positioned directly beneath the second impurity region. Accordingly, the proposed combination of references would not yield the claimed invention. Therefore, Applicant respectfully solicit the withdrawal of the imposed rejection of claim 8 under 35 U.S.C. § 103 for obviousness predicated upon Ueno in view of Hwang and further in view of Galbiati.

Claims 10 and 12-13 are rejected under 35 U.S.C. § 103 for obviousness predicated upon Ito, U.S. Patent No. 6,051,457, apparently in view of Chevalier, U.S. Patent No. 6,291,862

In the sixth enumerated paragraph of the statement of the rejection, the Examiner asserted that one having ordinary skill in the art would have been motivated to modify Ito with Chevalier to provide the teaching of a switching function and to operate in a depletion mode. This rejection is respectfully traversed.

Initially, Applicant notes that both claim 10 (similar to claim 1) has been amended to recite that the gap part is positioned directly beneath the second impurity region. In the semiconductor device shown in Fig. 2(h) of Ito, the second impurity region 26 is formed directly above the gap part of the buried impurity region 18. However, the second impurity region 26 is electrically connected through a P well 28 to the P+ buried impurity region 16. The P+ buried impurity region is arranged in the gap part, and therefore, the second impurity region 26 substantially extends to the region of the gap part. Thus, with the device of Ito, the breakdown voltage would be limited between the N+ buried impurity region 18 and the P+ buried impurity region. In the present invention, the second impurity region 35 does not extend to the position of the gap part. Accordingly, the present invention further improves the breakdown voltage as compared with the Ito reference. Furthermore, Applicant notes that below the N+ buried impurity region 18 of Ito, and N- impurity region of the same conductivity is formed. In contrast, a region of the opposite conductivity type (P type region of the semiconductor substrate) is positioned below the buried impurity region of the present invention. Thus, the present invention distinguishes from Ito. Applicant, therefore, respectfully submits that the imposed rejection of claims 10 and 12-13 under 35 U.S.C. § 103 for obviousness predicated upon Ito is not viable and, hence, solicits withdrawal thereof.

With regard to claim 12, in which the Examiner is puzzled over the terminology "fourth impurity region" when only two impurity regions are recited in claim 10, the Examiner is directed to claim 11, which recites a third and fourth impurity regions. By reciting a fourth impurity region in claim 12, Applicant has merely maintained consistency in claim terminology between like elements recited in claims 11 and 12.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

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Version with markings to show changes made

IN THE CLAIMS:

Please amend claims 1 and 10 as follows:

1. (Amended) A semiconductor device including:

a semiconductor substrate having a main surface;

a semiconductor layer of a first conductive type which is formed on the main surface of said semiconductor substrate;

a first buried impurity region of the first conductive type formed between said semiconductor layer and said semiconductor substrate;

a second buried impurity region of a second conductive type formed between said first buried impurity region and said semiconductor layer;

a first impurity region of the second conductive type which is formed in the surface of said semiconductor layer and which is electrically connected to said second buried impurity region;

a second impurity region of the first conductive type which is formed in the surface or inside of said semiconductor layer located in a region above said second buried impurity region; and

a semiconductor element which includes said first impurity region and said second impurity region and which has a switching function formed on the surface of said semiconductor layer,

wherein the withstanding voltage is secured by a depletion layer extending from an interface between said second buried impurity region and said semiconductor layer under the condition where said semiconductor element is turned OFF; and

said second buried impurity region includes a first gap part wherein said second buried impurity region is disconnected, said gap part of the second buried impurity region positioned directly beneath said second impurity region.

10. (Amended) A semiconductor device including:

a semiconductor substrate having a main surface;

a semiconductor layer of a first conductive type formed on the main surface of said semiconductor substrate;

a buried impurity region of the first conductive type formed between said semiconductor substrate and said semiconductor layer;

a first impurity region of the first conductive type which is formed on the surface of said semiconductor layer and which is electrically connected to said buried impurity region;

a second impurity region of a second conductive type formed on a surface of said semiconductor layer located in a region above said buried impurity region; and

a semiconductor element which includes said first impurity region and said second impurity region and which has a switching function formed on the surface of said semiconductor layer,

wherein a withstanding voltage is secured by a depletion layer extending from an interface between said second impurity region and said semiconductor layer under the condition where said semiconductor element is turned off; and

said buried impurity region includes a gap part wherein said buried region is disconnected, said gap part of the second buried impurity region positioned directly beneath said second impurity region.